

CLAIMS:

1. A Finite Impulse Response (FIR) filter device for sample rate converting a sequence of discrete representations; the filter device including:
 - an input pipeline IP for receiving the sequence of discrete representations and including:
 - 5 - a sequence of input delay cells DI_i , each for storing a discrete representation; and
 - a plurality of N input tap points TP_i , where an input tap point is provided at least between each sequential pair of input delay cells;
 - an output pipeline for supplying a sequence of discrete representations and including:
 - 10 - a sequence of output delay cells DO_i , each for storing a discrete representation;
 - a plurality of N summing elements S_i for adding at least two discrete representations, a summing element being provided at least between each sequential pair of output delay cells; and
 - 15 - an output switching network OSN for accumulating output values from the summing elements; and
 - a sequence of N taps T_i for coupling the input pipeline to the output pipeline; each tap including a respective multiplier M_i for multiplying a discrete representation from an input tap point by a coefficient; at least $N-1$ of the taps including a switching element for directing a discrete representation from an input tap point through the multiplier to a summing element; the switching elements being arranged to enable supply of a discrete representation from any tap point TP_j to a summing element S_i , where $j \leq i$.
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- 25 2. A FIR filter device as claimed in claim 1, wherein each of the taps T_i are coupled to only one respective summing elements S_i ; the switching element SW_i being provided in between tap points TP_j , where $j \leq i$ and the multiplier M_i .

3. A FIR filter device as claimed in claim 1, having a constant filter width N , N output delay cells DO_i , and N or $N-1$ input delay cells DI_i .
4. A FIR filter device as claimed in claim 1, wherein the input pipeline includes a
5 input switching network ISN for accumulating input values in the input delay cells DI_i .
5. A FIR filter device as claimed in claim 1, wherein each multiplier M_i is associated with a respective coefficient matrix C_i to enable poly-phase filtering.
- 10 6. A FIR filter device as claimed in claim 1, including a controller operative to control the filter device based on a state machine.
7. A FIR filter device as claimed in claim 1, wherein the state machine determines at least one of the following:
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 - a setting of the switching elements SW_i ,
 - a setting of the output switching network,
 - clocking of the input pipeline and/or output pipeline.
8. A FIR filter device as claimed in claim 5 and 7, wherein the state machine
20 determines selection of a coefficient from the coefficient matrix C_i .
9. A FIR filter device as claimed in claim 4 and 7, wherein the state machine determines a setting of the input switching network.
- 25 10. A FIR filter device as claimed in claim 1, including a further delay element and a subtracting element for determining a difference between an input discrete element and an immediately preceding input discrete element and supplying the difference into the input pipeline; and including a further summing element for adding input discrete element or the immediately preceding input discrete element to an output discrete element to be supplied by
30 the output pipeline.
11. A signal processing apparatus including a FIR filter device as claimed in claim 1 for sample rate converting an input signal, where the discrete representation is a sampled input signal, for subsequent rendering by a rendering device.

12. A signal processing apparatus as claimed in claim 11, wherein the signal processing apparatus includes the rendering device.